Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A method of forming an antifuse on a semiconductor substrate, the method comprising:

providing a partially formed semiconductor device having a substrate;

implanting nitrogen into a first portion of the substrate of an unmasked portion of the partially formed semiconductor device;

implanting a second portion of the substrate with nitrogen;

using a wet oxidation process to simultaneously grow [[ing]] a **first** dielectric oxide layer on the nitrided first portion of the substrate ~~using a wet oxidation process~~ **and to grow a second dielectric oxide layer on the nitrided second portion of the substrate wherein the thickness of the first dielectric oxide layer is different than the thickness of the second dielectric oxide layer**; and

depositing a gate material directly on the dielectric oxide layer, wherein the gate material comprises one terminal of the antifuse.

Claim 2 (original): The method of forming an antifuse as recited in claim 1, wherein the nitrogen is implanted using a dose in the range from about 5×10^{13} atoms/cm^2 to 1×10^{15} atoms/cm^2 of nitrogen.

Claim 3 (original): The method of forming an antifuse as recited in claim 1, wherein the nitrogen is implanted using an energy in the range from about 5 to 50 Kev.

Claim 4 (currently amended): The method of forming an antifuse as recited in claim 1, wherein the nitrogen implant dose is about 4×10^{14} atoms/cm^2 implanted at an energy **in the range** of about **5 keV to about 50 keV.** ~~25 Kev.~~

Claim 5 (original): The method of forming an antifuse as recited in claim 1, wherein the wet oxidation process takes place at a temperature in the range from 800 to 900 degrees C.

Claim 6 (original): The method of forming an antifuse as recited in claim 1, wherein a sacrificial oxide layer is first grown on the substrate and the nitrogen is implanted within 200-600 Angstroms of the interface between the sacrificial oxide and the substrate.

Claim 7 (original): The method of forming an antifuse as recited in claim 1, wherein the thickness of the grown dielectric oxide layer is in the range from 30 to 40 Angstroms.

Claim 8 (original): The method of forming an antifuse as recited in claim 1, wherein the thickness of the grown dielectric oxide layer is in the range from 40 to 60 Angstroms.

Claim 9 (cancelled)

Claim 10 (currently amended): The method of forming an antifuse as recited in claim 1 [[9]], wherein the dose of the nitrogen in the second portion is different than the dose in the first portion.

Claim 11 (currently amended): A method of determining the programmed state of an antifuse formed on a semiconductor substrate, the method comprising:

implanting nitrogen into a first portion of the substrate;

growing an oxide dielectric layer on the nitrided first portion using a wet oxidation process **that exposes the nitrided first portion to an ambient consisting of water**;

forming a patterned gate on the oxide dielectric layer to form the gate node of the antifuse;

forming at least one active region in the substrate, wherein the at least one active region is coupled to a ground voltage to form a ground node and arranged with the oxide dielectric and patterned gate to form the antifuse having the gate node and the ground node;

coupling the gate node to a voltage supply; and

determining the programmed state of the antifuse by sensing the voltage or current at the gate node.

Claim 12 (original): The method of determining the programmed state of an antifuse as recited in claim 11, wherein the gate node is switchably coupled to the voltage supply.

Claim 13 (original): The method of determining the programmed state of an antifuse as recited in claim 11, wherein a transistor is connected in series between the voltage supply and the gate node and a switchable connection between the voltage supply and gate node is controlled by a voltage input provided to the gate of the transistor.

Claim 14 (original): The method of determining the programmed state of an antifuse as recited in claim 11, wherein sensing the voltage or current at the gate node includes electrically connecting the gate node to a sense amplifier.

Claim 15 (original): The method of determining the programmed state of an antifuse as recited in claim 11, wherein the antifuse is programmable by the application of a second voltage between the gate node and the ground node and wherein the second voltage is higher than the supply voltage.

Claim 16 (cancelled)

Claim 17 (cancelled)

Claim 18 (cancelled)

Claim 19 (new): A method of forming an antifuse on a semiconductor substrate, the method comprising:

providing semiconductor substrate having a plurality of shallow isolation trenches that define active regions between the trenches;

selectively implanting nitrogen into a first active region of the substrate;

exposing the nitrogen implanted active region to an oxidizing ambient consisting of water thereby growing an oxide layer on the nitrogen implanted active region; and

forming a gate directly on the oxide layer, wherein the gate comprises one terminal of the antifuse device.

Claim 20 (new): The method of Claim 19 wherein exposing the nitrogen implanted active region to an oxidizing ambient includes an ambient consisting of H and OH radicals.

Claim 21 (new): The method of Claim 19, further comprising selectively implanting nitrogen into a second active region of the substrate and exposing the nitrogen implanted second active region to the oxidizing ambient at the same time as the oxide layer to form a second oxide layer having a thickness different than the oxide layer.